1. A process for planarizing an integrated circuit structure comprising at least one dielectric layer on a silicon substrate, said dielectric layer having openings therein lined with a layer of electrically conductive barrier material and filled with copper filler material, said process consisting essentially of:

a) removing, by a chemical mechanical polish (CMP) process step, a portion of the excess copper filler material over the portion of an electrically conductive barrier layer lying on the upper surface of said dielectric layer;

b) removing, by an electropolishing process step, the remainder of said excess copper filler material over said portion of said electrically conductive barrier layer lying on said upper surface of said dielectric layer to thereby expose said underlying electrically conductive barrier layer on said upper surface of said dielectric layer; and

c) then removing exposed portions of said electrically conductive barrier layer on said upper surface of said dielectric layer in a dry etch reactor using a plasma etching process selective to said copper and said dielectric layer until all of said portions of said electrically conductive barrier layer over said upper surface of said dielectric layer are removed;

whereby said integrated circuit structure may be planarized by removal of all of said copper layer and said electrically conductive barrier layer from said upper surface of said dielectric layer while inhibiting dishing and/or erosion of the surface of said copper filler material in said openings dielectric layer.

2. The process of claim 1 wherein the amount of copper removed by said chemical mechanical polish (CMP) process step to remove sufficient excess copper (formed over the barrier liner portions on the top surface of the dielectric layer) to provide a planarized layer of excess copper with a global planarity of about 20 nm to about 30 nm.

3. The process of claim 2 wherein said dielectric layer comprises a layer of low k dielectric material.

4. The process of claim 2 wherein said silicon substrate, having said dielectric layer thereon, said barrier liner over said dielectric layer, and said excess copper thereon to be removed by said electropolishing process step, is immersed in an electrolytic bath of chemical reagents.

5. The process of claim 4 wherein said silicon substrate having said dielectric layer thereon, said barrier liner over said dielectric layer, and said excess copper thereon to be removed by said electropolishing process, is electrically connected to the positive electrode (anode) of a DC power supply.

6. The process of claim 5 wherein a counter electrode is also mounted in said electrolytic bath and said counter electrode is electrically connected to the negative electrode of said DC power supply.

7. The process of claim 6 wherein said DC power supply is capable of providing a DC voltage range of from about 0.5 volts DC to about 5 volts DC.

8. The process of claim 7 wherein said excess copper is removed from said barrier liner on said surface of said dielectric layer by said electropolishing process during a period of from about 10 seconds to about 10 minutes while maintaining, between said silicon substrate and said counter electrode, a DC potential ranging from about 0.5 volts to about 5 volts

9. The process of claim 7 wherein said excess copper is removed from said barrier liner on said surface of said dielectric layer by said electropolishing process during a period of from about 10 seconds to about 5 minutes while maintaining, between said silicon substrate and said counter electrode, a DC potential ranging from about 0.5 volts to about 5 volts.

10. The process of claim 2 wherein, after removal of said excess copper, said barrier liner is removed from said upper surface of said dielectric layer by contacting said exposed portions of said barrier liner, in a dry etch reactor, with a plasma ignited while flowing through said dry etch reactor one or more gases selected from the group consisting of $Cl_2$, $CF_4$, $SF_6$, $C_4F_8$, and $BCl_3$.

11. The process of claim 10 wherein said plasma is maintained at a power level ranging from about 5 watts to about 1500 watts.

12. The process of claim 11 wherein said reactor is maintained within a pressure range of from about 3 millitorr to about 1000 millitorr during said dry etch process.

13. The process of claim 12 wherein the temperature of said integrated circuit substrate is at least about -50°C during said dry etching process.

14. The process of claim 12 wherein the temperature of said integrated circuit substrate does not exceed about 200°C during said dry etching process.

15. The process of claim 10 wherein said etching of said barrier liner material is monitored monochromatically to determine the endpoint when all of the barrier liner material on the top surface of said dielectric layer has been removed.

16. A process for planarizing an integrated circuit structure comprising at least one low k dielectric layer on a silicon substrate having openings therein comprising vias and trenches lined with a layer of electrically conductive barrier liner material and filled with copper filler material which process comprises:

a) removing, by a chemical mechanical polish (CMP) first process step, a portion of the excess copper filler material over the portion of an electrically conductive barrier layer lying on the upper surface of said low k dielectric layer;

b) removing, by an electropolishing second process step, the remainder of said excess copper filler material over said portion of said electrically conductive barrier layer lying on said upper surface of said low k dielectric layer, b:

i) immersing said silicon substrate in an electrolytic bath;

ii) electrically connecting said silicon substrate to the positive electrode (anode) of a DC power supply;

iii) electrically connecting a counter electrode in said electrolytic bath to the negative electrode of said DC power supply to commence said electropolishing process; and

iv) maintaining, between said silicon substrate and said counter electrode, a DC potential ranging from about 0.5 volts to about 5 volts for a period of from about 10 seconds to about 10 minutes to thereby remove the remainder of said copper over said barrier line on the top surface of said low k dielectric layer, and to expose said underlying electrically conductive barrier layer on said upper surface of said low k dielectric layer; and

c) then removing, in a dry etch reactor, exposed portions of said electrically conductive barrier layer on said upper surface of said dielectric layer in a third plasma etching process step selective to said copper and said dielectric layer until all of said portions of said electrically conductive barrier layer over said upper surface of said dielectric layer are removed, said plasma etching step further comprising:

i) contacting said exposed portions of said barrier liner, in said dry etch reactor, with a plasma ignited while flowing through said dry etch reactor one or more gases selected from the group consisting of $Cl_2$, $CF_4$, $SF_6$, $C_4F_8$, and $BCl_3$. while maintaining said plasma at a power level ranging from about 5 watts to about 1500 watts, and said reactor within a pressure range of from

about 3 millitorr to about 1000 millitorr, and a temperature of at least about -50°C but not exceeding about 200°C during said dry etching process; and

ii) monitoring said etching of said barrier liner material to determine the endpoint when all of said barrier liner material on the top surface of said dielectric layer has been removed.

17. A process for planarizing an integrated circuit structure comprising at least one dielectric layer having openings therein lined with a layer of electrically conductive barrier material and filled with copper filler material which comprises:

a) removing, by a chemical mechanical polish process step, excess copper over the portion of an electrically conductive barrier layer lying on the upper surface of a dielectric layer until the underlying electrically conductive barrier layer on said upper surface of said dielectric layer is exposed; and

b) then removing exposed portions of said electrically conductive barrier layer on said upper surface of said dielectric layer in a reactor using a dry etching process selective to said copper and said dielectric layer until all of said portions of said electrically conductive barrier layer over said upper surface of said dielectric layer are removed; whereby said integrated circuit structure may be planarized by removal of all of said copper layer and said electrically conductive barrier layer from said upper surface of said dielectric layer while inhibiting dishing and/or erosion of the surface of said copper filler material in said openings.

18. The process of claim 17 wherein said dry etching process further comprises contacting said exposed portions of said barrier layer with a plasma ignited while flowing through said reactor one or more gases selected from the group consisting of $Cl_2$, $CF_4$, $SF_6$, $C_4F_8$, and $BCl_3$.

19. The process of claim 18 wherein said plasma is maintained at a power level ranging from about 5 watts to about 1500 watts.

20. The process of claim 19 wherein said reactor is maintained within a pressure range of from about 3 millitorr to about 1000 millitorr during said dry etch process.

21. The process of claim 20 wherein the temperature of said integrated circuit substrate is at least about -50°C during said dry etching process.

22. The process of claim 20 wherein the temperature of said integrated circuit substrate does not exceed about 200°C during said dry etching process.

23. The process of claim 18 wherein said etching of said barrier liner material is monitored monochromatically to determine the endpoint when all of the barrier liner material on the top surface of said dielectric layer has been removed.

24. The process of claim 17 wherein said dielectric layer further comprises a low k dielectric layer.

25. The process of claim 17 wherein said openings in said dielectric layer comprise trenches and said copper filler material in said trenches form a layer of copper interconnects.

26. A process for planarizing an integrated circuit structure comprising a dielectric layer having trenches therein lined with a layer of electrically conductive barrier material and filled with copper filler material which comprises:

a) providing a dielectric layer having a plurality of trenches formed therein;

b) depositing a barrier layer of electrically conductive material on exposed surfaces of said trenches and the top surface of said dielectric layer;

c) filling said trenches by depositing a layer of copper over said electrically conductive barrier layer;

d) removing excess copper over the portion of an electrically conductive barrier layer lying on said top surface of said dielectric layer by a chemical mechanical polish (CMP) process step selective to both said electrically conductive barrier layer and said dielectric layer until all of said copper on said electrically conductive barrier layer over said top surface of said dielectric layer is removed; and

e) then removing said exposed electrically conductive barrier layer on said top surface of said dielectric layer in a reactor using a dry etching process selective to said copper and said dielectric layer until all of said electrically conductive barrier layer on said top surface of said dielectric layer is removed;

whereby said integrated circuit structure may be planarized by removal of all of said copper layer and electrically conductive barrier liner from said top surface of said dielectric layer while inhibiting dishing and/or erosion of the surface of said copper in said trenches.

27. The process of claim 26 wherein said dielectric layer comprises a layer of low k dielectric material.

28. The process of claim 26 wherein said dry etching process further comprises contacting said exposed portions of said barrier layer with a plasma ignited while flowing through said reactor one or more gases selected from the group consisting of $Cl_2$, $CF_4$, $SF_6$, $C_4F_8$, and $BCl_3$.

29. The process of claim 28 wherein said plasma is maintained at a power level ranging from about 5 watts to about 1500 watts.

30. The process of claim 29 wherein said reactor is maintained within a pressure range of from about 3 millitorr to about 1000 millitorr during said dry etch process.

31. The process of claim 30 wherein the temperature of said integrated circuit substrate is at least about -50°C during said dry etching process.

32. The process of claim 30 wherein the temperature of said integrated circuit substrate does not exceed about 200°C during said dry etching process.

33. The process of claim 10 wherein said etching of said barrier liner material is monitored monochromatically to determine the endpoint when all of said barrier liner material on said top surface of said dielectric layer has been removed.

34. A process for planarizing an integrated circuit structure comprising a dielectric layer having trenches therein lined with a layer of electrically conductive barrier material and filled with copper filler material which comprises:

a) providing a first dielectric layer having a plurality of trenches formed therein, and a second dielectric layer below said first dielectric layer, said second dielectric layer having a plurality of vias therein, at least a portion of which are aligned with said trenches in said first dielectric layer;

b) depositing an electrically conductive barrier layer on exposed surfaces of said trenches and said vias, and over the top surface of said first dielectric layer;

c) filling said trenches and said vias by depositing a layer of copper over said electrically conductive barrier layer, including that portion of said electrically conductive barrier layer over said top surface of said first dielectric layer;

d) removing, by a chemical mechanical polish process step, excess copper over the portion of said electrically conductive barrier layer lying on said top surface of said first dielectric layer by a chemical mechanical polish process step selective to both said electrically conductive barrier layer and said dielectric layer until the all of said copper on said electrically conductive barrier layer over said top surface of said first dielectric layer is removed; and

e) then removing said exposed electrically conductive barrier layer on said top surface of said first dielectric layer in a reactor using a dry etching process selective to said copper and said dielectric layer until all of said electrically conductive barrier layer on said top surface of said first dielectric layer is removed;

whereby said integrated circuit structure may be planarized by removal of all of said copper layer and said electrically conductive barrier layer from said top surface of said first dielectric layer while inhibiting dishing and/or erosion of the surface of said copper in said trenches.

35. The process of claim 34 wherein said first dielectric layer and said second dielectric layer each comprise a layer of low k dielectric material.

36. In a process for forming a damascene structure of an integrated circuit structure wherein openings in one or more layers of low k dielectric materials are filled with one or more electrically conductive materials and excess portions of said electrically conductive materials are removed from the upper surface of said one or more low k dielectric layers, the improvement which comprises:

a) electropolishing the excess portions of said electrically conductive materials over said upper surface of said one or more low k dielectric layers to remove at least some of said excess electrically conductive materials; and

b) removing, by a subsequent plasma etching step, any of said excess portions of said electrically conductive materials not removed from the upper surface of said one or more low k dielectric layers by said electropolishing step.

37. The process of claim 36 wherein said electrically conductive materials comprise at least one electrically conductive diffusion barrier liner formed on surfaces of said openings and over said upper surface of said one or more low k dielectric layer and a layer of copper formed over said electrically conductive diffusion barrier liner.

38. The process of claim 37 wherein substantially all of said copper over said electrically conductive diffusion barrier liner over said upper surface of said one or more low k dielectric layers is removed by said electropolishing step.

39. The process of claim 38 wherein all of said electrically conductive diffusion barrier liner remaining over said upper surface of said one or more low k dielectric layers after said electropolishing step is removed by said subsequent plasma etching step.

40. The process of claim 39 wherein said diffusion barrier liner removed by said plasma etching step is selected from the group including, but not limited to the following materials: tantalum, tantalum nitride, titanium silicon nitride, tungsten, tungsten nitride, titanium, titanium nitride, and manganese dioxide.

41. The process of claim 40 wherein said diffusion barrier liner removed by said plasma etching step is selected from the group consisting of tantalum, tantalum nitride, titanium silicon nitride, tungsten, tungsten nitride, titanium, titanium nitride, and manganese dioxide.

42. The process of claim 41 wherein said diffusion barrier liner removed by said plasma etching step comprises tantalum,

43. The process of claim 36 wherein said electrically conductive materials consists essentially of copper and at least one electrically conductive diffusion barrier liner formed on surfaces of said openings and over said upper surface of said one or more low k dielectric layers;

i) wherein substantially all of said copper over said electrically conductive diffusion barrier liner over said upper surface of said one or more low k dielectric layers is removed by said electropolishing step; and

ii) wherein any remaining copper and all of said electrically conductive diffusion barrier liner remaining over said upper surface of said one or more low k dielectric layers after said electropolishing step is removed by said subsequent plasma etching step.

44. In a process for forming a damascene structure of an integrated circuit structure wherein openings in one or more layers of low k dielectric materials are lined with one or more layers of diffusion barrier liner; then filled with copper; and excess portions of said one or more layers of said diffusion barrier liner and said copper are removed from the upper surface of said one or more low k dielectric layers, the improvements which comprise:

a) electropolishing said excess portions of at least said copper over said upper surface of said one or more low k dielectric layers to remove said excess copper; and

b) then removing, by plasma etching, any excess portions of said one or more layers of diffusion barrier liner remaining over said upper surface of said one or more low k dielectric layers.

45. The process of claim 44 wherein said diffusion barrier liner removed by said plasma etching step is selected from the group including, but not limited to the following materials: tantalum, tantalum nitride, titanium silicon nitride, tungsten, tungsten nitride, titanium, titanium nitride, and manganese dioxide.

46. The process of claim 44 wherein said diffusion barrier liner removed by said plasma etching step is selected from the group consisting of tantalum, tantalum nitride, titanium silicon nitride, tungsten, tungsten nitride, titanium, titanium nitride, and manganese dioxide.

47. The process of claim 44 wherein said diffusion barrier liner removed by said plasma etching step comprises tantalum,;

d) removing, by a chemical mechanical polish (CMP) process step, excess copper over the portion of said electrically conductive barrier layer lying on said top surface of said first dielectric layer by a chemical mechanical polish process step selective to both said electrically conductive barrier layer and said dielectric layer until all of said copper on said electrically conductive barrier layer over said top surface of said first dielectric layer is removed; and

e) then removing said exposed electrically conductive barrier layer on said top surface of said first dielectric layer in a reactor using a dry etching process selective to said copper and said dielectric layer until all of said electrically conductive barrier layer on said top surface of said first dielectric layer is removed;

whereby said integrated circuit structure may be planarized by removal of all of said copper layer and said electrically conductive barrier layer from said top surface of said first dielectric layer while inhibiting dishing and/or erosion of the surface of said copper in said trenches.